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(71)Applicant : **KOMATSU LTD**

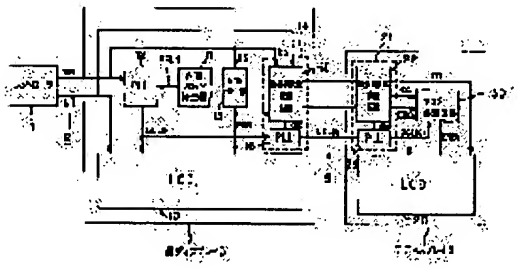
(72)Inventor : **TAKEBE SHIN**

(54) FLAT DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To transmit a display signal to a distant place and to normally display a picture by executing timedivision multiplex transmission based on a clock signal phasesynchronized with a digital system.

SOLUTION: At the time of receiving a horizontal synchronizing signal HS1 and an enable signal ENB1 by a slave display 5, these signals HS1, ENB1 include turbulence sections. The logcally inverted output of the signal HSI is inputted to the clock terminal of a flip flop (FF) in a mask processing circuit 30 and an output signal MASH is turned to 'L' when the signal HS1 falls. Since the logically inverted output of an output from a counter is inputted to the set terminal of the FF, the output signal MASH is turned to 'H' when the output of the counter rises. An AND circuit in the circuit 30 masks the enable signal ENB1 by the mask signal MASH to remove a signal turbulence section from the signal ENB1 and outputs an enable signal ENB2 free from signal turbulence to an LCD 20.



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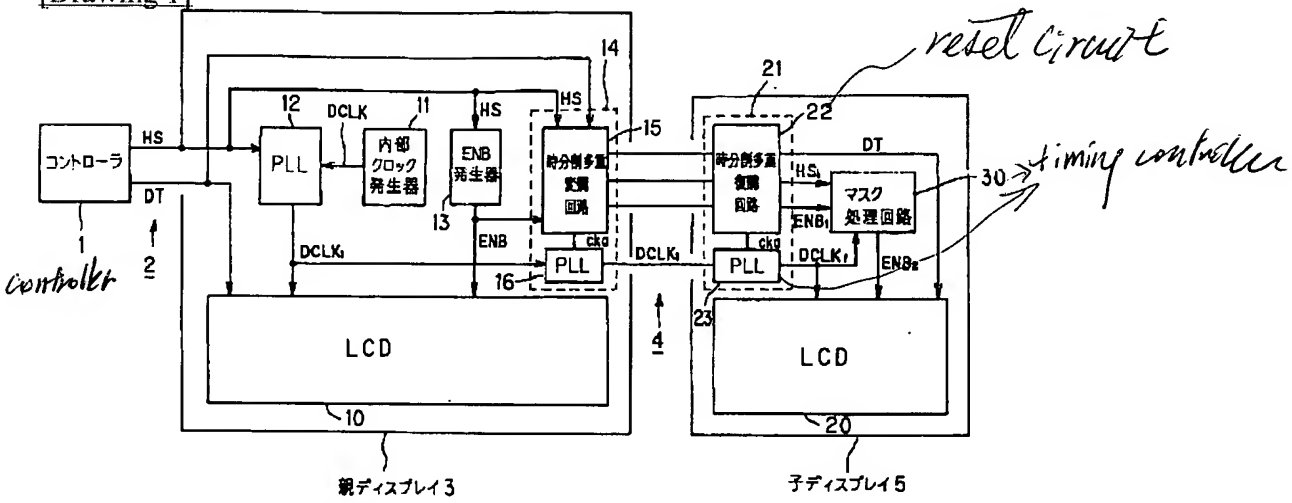
* NOTICES *

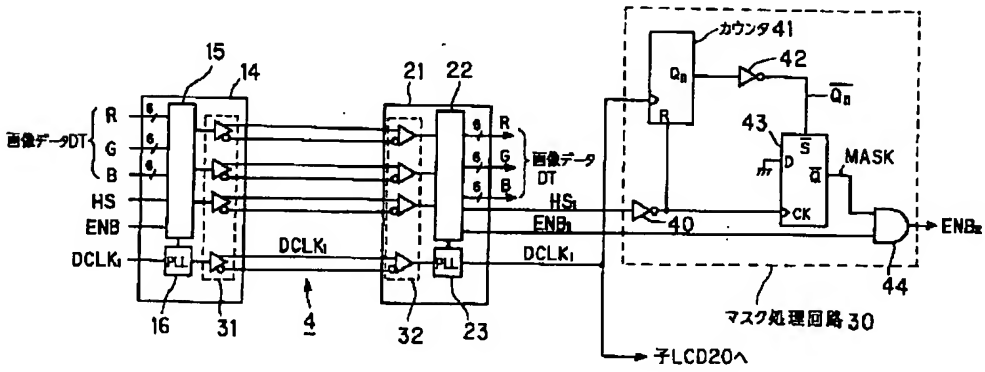
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

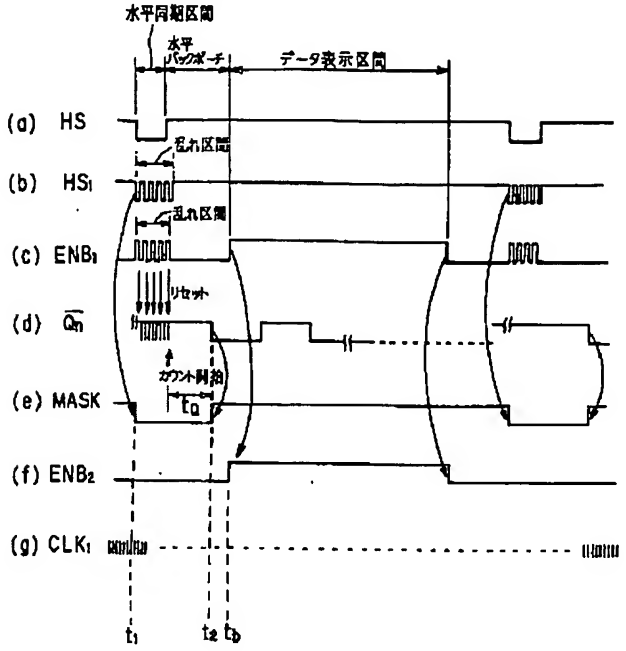
[Drawing 1]



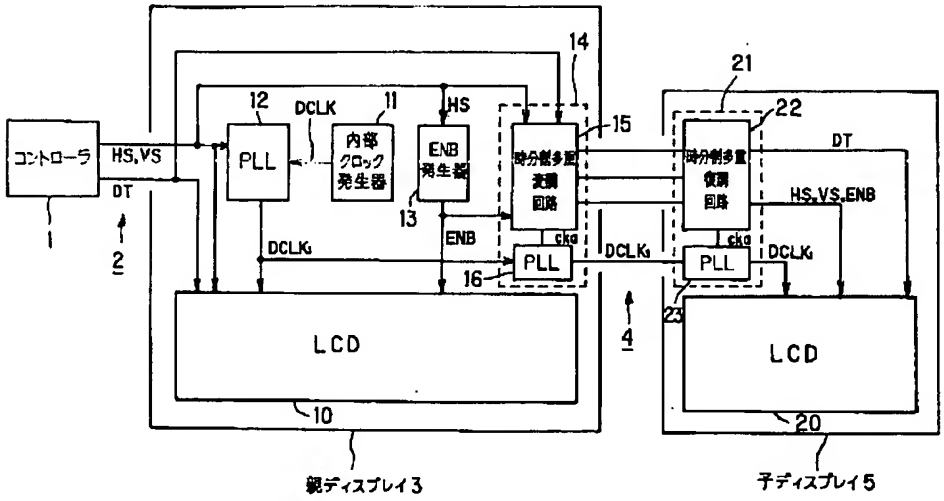
[Drawing 2]



[Drawing 3]



[Drawing 4]



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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the amelioration for canceling the poor display in the flat display which considered as the cause that it could not restore to the display synchronizing signal at the time of performing Time-Division-Multiplexing transmission using the clock signal for a display which the mustache, the jitter, etc. mixed especially by digital phase simulation processing about the flat display indicating equipment which transmits a status signal using time-division multiplexing, such as LDVS, and is displayed on flat displays, such as a liquid crystal display, by the receiving side.
[0002]
[Description of the Prior Art] In the facility device arranged at works etc., there is a case where the same contents of a display, such as various kinds of messages and actuation advice, are displayed on each indicator which has arranged flat indicators, such as a liquid crystal display, to two or more places, such as a side front, a background, etc. of a device, and has been arranged in the part of these plurality, plentifully.
[0003] In such a system, although status signals, such as display-image data and a display synchronizing signal, will be transmitted to each above-mentioned indicator from the Maine controller, the distance between these devices is usually greatly separated in many cases. For this reason, it enables it to make data transfer for the status signal which consists of many numbers of bits by transmitting a status signal using the data transmission by Time Division Multiplexing, such as LDVS specification (LOW VOLTAGE DIFFERENTIAL SIGNALLING), at a high speed with a low power with few signal lines in this kind of system.
[0004] The conventional image display system which used the above-mentioned LVDS method for drawing 4 is shown.
[0005] This image display system has the composition that the parent display unit 3 is connected to a controller 1 through a signal cable 2, and the child display unit 5 is connected to this parent display unit 3 through a signal cable 4.
[0006] From a controller 1, the color picture data DT, Horizontal Synchronizing signal HS, and Vertical Synchronizing signal VS of RGB are transmitted to the parent display 3.
[0007] In the parent display unit 3, the internal clock signal DCLK for a display over the liquid crystal display (it is called Following LCD) 10 of the parent display unit 3 and LCD20 of the child display 5 is generated by the internal clock generator 11. Phase simulation is performed by digital processing and a phase lock loop (henceforth a PLL circuit) 12 performs phase simulation control doubled with the phase of Horizontal Synchronizing signal HS into which the phase of the internal clock signal DCLK was inputted from the controller 1. That is, for example, phase simulation control which doubles the phase of the internal clock signal DCLK with the first transition section (for example, fall) of a Horizontal Synchronizing signal is performed. The ENB generator 13 forms the enable signal ENB which shows the period which displays image data actually based on Horizontal Synchronizing signal HS inputted from the controller 1. LCD10 of the parent display 3 performs a display action using inputted Horizontal Synchronizing signal HS, Vertical Synchronizing signal VS, enable signal ENB, the internal clock signal DCLK1, and the color picture data DT.
[0008] On the other hand, in order to carry out high-speed transmission of the status signal required for a display in the child display unit 5 to the child display unit 5, IC14 for Time-Division-Multiplexing transmission by LVDS specification is carried, and this IC14 is constituted from a Time-Division-Multiplexing modulation circuit 15 and a PLL circuit 16 by the parent display unit 3. The PLL circuit 16 transmits the internal clock signal DCLK1 inputted from the PLL circuit 12 to up to the signal cable 4 to the child display 5 while it generates the clock signal CKa for a high-speed modulation (a signal N times the frequency of DCLK) synchronized with the phase of the inputted internal clock signal DCLK1 and inputs this generated clock signal CKa into the Time-Division-Multiplexing modulation circuit 15. The Time-Division-Multiplexing modulation circuit 15 modulates indicative-data DT, Horizontal Synchronizing signal HS, Vertical Synchronizing signal VS, and enable signal ENB which were inputted based on the inputted clock signal CKa for a modulation to Time-Division-Multiplexing data, and transmits this modulation data to up to the signal cable 4 to the child display 5.
[0009] IC21 for the Time-Division-Multiplexing reception for restoring to the above-mentioned Time-Division-Multiplexing data to the original signal is carried in the child display unit 5, and this IC21

consists of a Time-Division-Multiplexing demodulator circuit 22 and a PLL circuit 23. The PLL circuit 23 inputs the received internal clock signal DCLK1 into LCD20 of the child display 5 while it generates the clock signal CKa for a recovery (a signal N times the frequency of DCLK1) synchronized with the phase of the inputted internal clock signal DCLK1 and inputs this generated clock signal CKa into the Time-Division-Multiplexing demodulator circuit 22. The Time-Division-Multiplexing demodulator circuit 22 restores to the Time-Division-Multiplexing data received based on the inputted clock signal CKa for a recovery to original indicative-data DT, Horizontal Synchronizing signal HS, Vertical Synchronizing signal VS, and an enable signal ENB, and inputs into LCD20 of the child display 5 this data to which it restored.

[0010] LCD20 of the child display 5 performs a display action using inputted Horizontal Synchronizing signal HS, Vertical Synchronizing signal VS, enable signal ENB, the internal clock signal DCLK1, and the color picture data DT. Thereby, parents and the same display image as each LCD 10 and 20 of the child displays 3 and 5 can be displayed simultaneously.

[0011]

[Problem(s) to be Solved by the Invention] However, in the image display system mentioned above, in case the phase of the internal clock signal DCLK is doubled with the phase of Horizontal Synchronizing signal HS in the PLL circuit 12 (in first transition section), a jitter (phase variation rate) may occur to the internal clock signal DCLK, a mustache may occur at the change of a clock, or the discontinuous condition of a clock may occur.

[0012] However, in this image display system, it sets in IC14 for transmission, and IC21 for reception. The object for a modulation and the clock signal CKa for a recovery which carried out phase simulation to the internal clock signal DCLK1 which the jitter, the mustache, etc. generated in the PLL circuits 16 and 23 are formed. Since it is made to perform the Time-Division-Multiplexing modulation and recovery processing which were synchronized with this clock signal CKa using the these-formed clock signal CKa In Horizontal Synchronizing signal HS and enable signal ENB which are outputted from IC21 for reception The problem that the image which the turbulence period when H and L become random from the event (at for example, the fall event) of Horizontal Synchronizing signal HS becoming effective a little in between occurs, consequently is displayed by the parent display 3 side was not displayed at all by LCD20 by the side of the child display 5 occurred.

[0013] That is, by this system, since 2 times, 3 times, and phase simulation are performed in the PLL circuits 16 and 23 and Time-Division-Multiplexing modulation and recovery processing are performed based on the clock signal from which that synchronization may separate and this synchronization separated on the basis of the internal clock signal which the jitter outputted from the PLL circuit 12 and the mustache have generated, it is thought that a turbulence period arises in Horizontal Synchronizing signal HS or an enable signal ENB.

[0014] In addition, since he is trying for the turbulence of the signal generated in Horizontal Synchronizing signal HS and enable signal ENB by the side of the child display unit 5 to double the phase of the internal clock signal DCLK in the PLL circuit 12 in the first transition section (for L to be a fall when effective) of Horizontal Synchronizing signal HS, as mentioned above, only a little between occurs from the fall event of Horizontal Synchronizing signal HS, and it is not generated during the data display section which is a shelf-life of an enable signal ENB.

[0015] Against such a problem, another IC for transmission and reception which does not perform time-division multiplexing other than ICs 14 and 21 for LVDS data transmission and reception which performs time-division multiplexing was prepared conventionally, and the cure of sending synchronizing signals for a display, such as enable signal ENB and Horizontal Synchronizing signal HS, to the child display 5 using these ICs was taken.

[0016] However, since IC which transmits ********** HS and an enable signal ENB, and IC which transmits image data and a clock signal are set aside according to this conventional technique, when the difference of the signal-transmission time amount between each [these] IC or apparent signal delay varies, gap of timing occurs to the signal of both ICs, and there is a problem that there is no nothing profit of a proper display action in the child display 5.

[0017] This invention is made in view of such the actual condition, and it aims at offering the flat display display which transmits a status signal to the location which distance left, and displays this by performing Time-Division-Multiplexing transmission by the clock signal which performed phase

simulation of a digital system and which hits and enabled it to display an image normally.
[0018]
[Means for Solving the Problem and its Function and Effect] Then, a clock generation means to generate the internal clock signal of a predetermined period in this invention, The 1st phase lock loop which doubles the phase of said internal clock signal with the phase of the Horizontal Synchronizing signal into which it is inputted from the exterior, The enable signal means forming which forms the enable signal which becomes the validity between the display periods of image data based on the display synchronizing signal inputted from the exterior, The 2nd phase lock loop which generates the clock signal for a modulation synchronized with the phase of the internal clock signal outputted from said 1st phase lock loop, The indicative data inputted based on the clock signal for a modulation generated from this 2nd phase lock loop, The sending circuit which has the transmitting section which transmits the internal clock signal outputted from the modulation circuit which modulates a Horizontal Synchronizing signal and said enable signal to Time-Division-Multiplexing data, and said 1st phase lock loop, and said modulated Time-Division-Multiplexing data, With the receive section which receives said internal clock signal and said Time-Division-Multiplexing data from said sending circuit The Time-Division-Multiplexing data received based on the clock signal for a recovery generated from the 3rd phase lock loop which generates the clock signal for a recovery synchronized with the phase of this received internal clock signal, and this 3rd phase lock loop The original indicative data, The receiving circuit which has the demodulator circuit to which it restores to a Horizontal Synchronizing signal and said enable signal, Based on the Horizontal Synchronizing signal outputted from this receiving circuit, answer the first transition section of a Horizontal Synchronizing signal, and it is turned on. The mask signal means forming which forms the mask signal which it is at the event after the trailing-edge section of the Horizontal Synchronizing signal concerned, and becomes off at the event before the first transition of the enable signal of the same line period as the Horizontal Synchronizing signal concerned, A mask-processing means to remove the signal part corresponding to the "on" period of a mask signal from said enable signal by carrying out mask processing of said enable signal outputted based on said mask signal from said receiving circuit, He is trying to have the internal clock signal and indicative data which are outputted from said receiving circuit, and the flat display which performs a predetermined display action based on the enable signal outputted from said mask-processing means.
[0019] This invention is applicable to the possible flat display of a display action, using only an enable signal as a display synchronizing signal. That is, in flat displays, such as the latest liquid crystal display, there are many models which can perform a display action, using only an enable signal as a synchronizing signal without using a Horizontal Synchronizing signal and a Vertical Synchronizing signal, and this invention can be applied to the flat display of such a model.
[0020] That is, as mentioned above, during some periods occurs from the first transition section (at for example, the fall event) of a Horizontal Synchronizing signal, and the turbulence of the signal generated in an enable signal is not generated during the data display section which is a shelf-life of an enable signal. Moreover, although turbulence of a signal generates during some periods from the first transition section (at for example, the fall event) in a Horizontal Synchronizing signal, there is no gap in the time amount timing of the first transition section of a Horizontal Synchronizing signal. That is, the timing of the first transition section of a Horizontal Synchronizing signal itself receives normally, and it is changeless.
[0021] This invention was made paying attention to such a point, and is based on a Horizontal Synchronizing signal including the above-mentioned turbulence section. The mask signal which answers the first transition section of a Horizontal Synchronizing signal, is turned on, and it is at the event after the trailing-edge section of the Horizontal Synchronizing signal concerned, and becomes off at the event before the first transition of an enable signal is formed. By removing the signal part corresponding to the "on" period of a mask signal from the enable signal which includes the turbulence section using this mask signal The cage which is made to perform the display action of a flat display, using the enable signal with which the turbulence section of an enable signal was eliminated and this turbulence section was eliminated as a synchronizing signal, When a status signal is transmitted to the location which distance left using time-division multiplexing by this and this is displayed, an image can be displayed on normal and stability.
[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0023] The block diagram of the image display system of this invention is shown in drawing 1 . Moreover, drawing 2 shows the internal configuration of IC for data transmission of drawing 1 , IC21 for data reception, and the mask-processing circuit 30.

[0024] A display action is possible for LCD10 and LCD20 of this image display system, using only an enable signal ENB as a display synchronizing signal, and Horizontal Synchronizing signal HS and Vertical Synchronizing signal VS are not used in the case of a display.

[0025] That is, in this system, it is made to perform the display action of LCD20 in the mask-processing circuit 30, using the enable signal ENB2 with which the signal turbulence section was eliminated from the enable signal ENB1 including the signal turbulence section using Horizontal Synchronizing signal HS1 and enable signal ENB1 including the turbulence section mentioned above, and this signal turbulence section was eliminated as a synchronizing signal.

[0026] Hereafter, a configuration and an operation of each part are explained in full detail.

[0027] From a controller 1, the color picture data DT and Horizontal Synchronizing signal HS of RGB are transmitted to the parent display unit 3.

[0028] In the parent display unit 3, the internal clock signal DCLK for a display over the liquid crystal display (it is called Following LCD) 10 of the parent display unit 3 and LCD20 of the child display 5 is generated by the internal clock generator 11. By DESHITARU processing, a phase lock loop (henceforth a PLL circuit) 12 performs phase simulation control which doubles the phase of the internal clock signal DCLK with the phase (fall) of Horizontal Synchronizing signal HS into which it was inputted from the controller 1, and inputs the output DCLK1 into LCD10 and the PLL circuit 16. The ENB generator 13 forms the enable signal ENB which shows the period which displays image data actually based on Horizontal Synchronizing signal HS inputted from the controller 1. LCD10 of the parent display 3 performs a display action using enable signal ENB and the internal clock signal DCLK1 which were inputted, and the color picture data DT.

[0029] IC14 for Time-Division-Multiplexing transmission by LVDS specification consists of a Time-Division-Multiplexing modulation circuit 15, a PLL circuit 16, and a driver line 31. The PLL circuit 16 transmits the internal clock signal DCLK1 inputted from the PLL circuit 12 through a driver line 31 to up to the signal cable 4 to the child display unit 5 while it generates the clock signal CKa for a high-speed modulation (a signal N times the frequency of DCLK) synchronized with the phase of the inputted internal clock signal DCLK1 and inputs this generated clock signal CKa into the Time-Division-Multiplexing modulation circuit 15. The Time-Division-Multiplexing modulation circuit 15 modulates the color display data DT, Horizontal Synchronizing signal HS, and enable signal ENB of RGB which were inputted based on the inputted clock signal CKa for a modulation to Time-Division-Multiplexing data, and transmits this modulation data through a driver line 32 to up to the signal cable 4 to the child display unit 5.

[0030] IC21 for Time-Division-Multiplexing reception carried in the child display unit 5 consists of a receiver circuit 32, a Time-Division-Multiplexing demodulator circuit 22, and a PLL circuit 23. The PLL circuit 23 outputs the received internal clock signal DCLK1 to LCD20 and the mask-processing circuit 30 of the child display 5 while it generates the clock signal CKa for a recovery (a signal N times the frequency of DCLK1) synchronized with the phase of the inputted internal clock signal DCLK1 and inputs this generated clock signal CKa into the Time-Division-Multiplexing demodulator circuit 22. The Time-Division-Multiplexing demodulator circuit 22 inputs Horizontal Synchronizing signal HS1 and an enable signal ENB1 into the mask-processing circuit 30 while it restores to the Time-Division-Multiplexing data received based on the inputted clock signal CKa for a recovery to the color display data DT, original Horizontal Synchronizing signal HS1, and original enable signal ENB1 of RGB and inputs into LCD20 of the child display 5 this indicative-data DT to which it restored.

[0031] The inverter 40 with which the mask-processing circuit 30 carries out the reversal output of Horizontal Synchronizing signal HS1 as shown in drawing 2 , The counter 41 which performs count actuation in which reversed Horizontal Synchronizing signal HS1_ (a logic reversal notation is outlined by _) was inputted into the reset terminal, and followed the internal clock signal DCLK1, The inverter 42 which carries out the reversal output of the 1-bit output Qn of a counter 41, The flip-flop 43 by which output Qn_ of an inverter 42 was inputted into the set terminal, the data terminal was grounded and

Horizontal Synchronizing signal HS1_ was inputted into the clock terminal, The AND of the mask signal MASK and the enable signal ENB1 which are outputted from a flip-flop 43 was taken, and it has AND gate 44 which outputs the output ~~ENB2 to~~ LCD20.

[0032] Next, actuation of the mask-processing circuit 30 is explained with reference to the timing chart of drawing 3 .

[0033] Here, as shown in drawing 3 (a), the signal turbulence section has not occurred in Horizontal Synchronizing signal HS before being inputted into the Time-Division-Multiplexing modulation circuit 15. However, as shown in drawing 3 (b) and (c), Horizontal Synchronizing signal HS1 and enable signal ENB1 in the phase received by the child display 5 side include the turbulence section for the reason mentioned above. During some periods occurs from the fall event (first transition section) of Horizontal Synchronizing signal HS1, and these turbulence sections do not occur during the data display section which is a shelf-life of an enable signal ENB1, as mentioned above. Moreover, there is no gap of timing at the fall event of the beginning of Horizontal Synchronizing signal HS1, and it is changeless to an all seems well.

[0034] Such a phenomenon is a premise when performing mask processing in the mask-processing circuit 30.

[0035] Since the logic reversal output of Horizontal Synchronizing signal HS1 is inputted into the clock terminal of the flip-flop 43 of the mask-processing circuit 30 and the data terminal is installed, the output signal MASK of a flip-flop 43 falls to "L (low)", when Horizontal Synchronizing signal HS1 falls (drawing 3 (e), time of day t1).

[0036] On the other hand, although a counter 41 is reset at the fall event of Horizontal Synchronizing signal HS1, since the condition that a signal falls to the signal turbulence section of Horizontal Synchronizing signal HS1 after that exists repeatedly, in connection with this, a counter 41 is reset repeatedly. Therefore, a counter 41 starts the original count actuation according to clock signal DCLK, when the turbulence section is completed. The output of a counter 41 starts [in / this sake / are trying to choose that from which, as for a counter 41, that output starts to t2 at the event before tb the event of choosing 1 bit of Qn(s), and being made to consider as that output, and a count initiation event to the enable signal ENB1 being set to "H (yes)" truly, as for that output Qn in n bits / of that original / output, and / time of day t2].

[0037] The output signal MASK of a flip-flop 43 takes action to "H" in the time of day t2 when the output of a counter 41 started to input the logic reversal output of the output of a counter 41 into the set terminal of a flip-flop 43.

[0038] Thus, from a flip-flop 43, when the output Qn of a counter 41 is set to "H" to "L" a fall and after that by t1 at the fall event of Horizontal Synchronizing signal HS1, the mask signal with which the output starts to "H" is outputted to t2 at the event before tb the event of the data display period of an enable signal ENB1 being started.

[0039] In AND circuit 44 of the mask-processing circuit 30, the signal turbulence section will be removed from the enable signal ENB2 which is made to carry out mask processing of the enable signal ENB1 with which the signal turbulence section is included, and is outputted by this by this mask signal MASK from AND circuit 44.

[0040] In addition, if the period tQ after a counter 41 is reset eventually until the output Qn starts to "H" excels rather than the turbulence section of a signal, the display by LCD20 can be ensured.

[0041] Thus, from the fall of Horizontal Synchronizing signal HS1 to the period of the middle of the level back porch, or the second half, the mask of the signal turbulence section of an enable signal ENB1 is carried out, and he removes it using mask signal MASK which is "L", and is trying to output the enable signal ENB2 without signal turbulence to LCD20 with this operation gestalt. Therefore, in LCD20, a normal display action becomes possible.

[0042] In addition, the fall event of the beginning of Horizontal Synchronizing signal HS1 is caught using the fall event of the output of a flip-flop 43, and you may make it make a counter 41 start count actuation from the fall event of the beginning of this Horizontal Synchronizing signal HS1 in the above-mentioned operation gestalt.

[0043] Moreover, although the above-mentioned operation gestalt showed the case where it was displayed on the same data said time of day as parent and child's display, you may make it apply this invention to a system so that a status signal may be transmitted to the location which distance left using

time-division multiplexing and this may be displayed.
[0044] Moreover, as long as a function equivalent to what was shown in the above-mentioned operation gestalt is attained about the mask-processing circuit 30, you may make it adopt the circuitry of other arbitration.